Amendments To The Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Currently Amended) A method for generating an optimized circuit that implements a program implemented in programmable logic, the method comprising:

generating a programmable logic circuit that implements a program;

analyzing [[a]] the programmable logic circuit ~~implemented in the programmable logic~~ for ~~possible~~ optimizations, wherein the analyzing comprises determining whether to split the program into a hardware portion implemented in the programmable logic circuit and a software portion implemented in at least one software processor; ~~and~~

optimizing the programmable logic circuit into the optimized circuit to provide a more efficient implementation of the program by modifying the programmable logic circuit to ~~executing a~~ execute the software portion of the program ~~using software constructs, wherein using software constructs comprises~~ on the at least one software processor; and

establishing communications between the optimized programmable logic circuit and the at least one software ~~device~~ processor.

2. (Currently Amended) The method of claim 1 wherein analyzing the programmable logic circuit comprises using a software-to-hardware compiler to analyze the programmable logic circuit at a later stage in a compilation.

3. (Currently Amended) The method of claim 1 wherein analyzing the programmable logic circuit comprises analyzing the programmable logic circuit's critical path.

4. (Currently Amended) The method of claim 1 wherein optimizing the programmable logic circuit comprises placing at least one register in the programmable logic circuit.

5. (Currently Amended) The method of claim 1 wherein optimizing the programmable logic circuit comprises placing at least one FIFO in the programmable logic circuit.

6. (Currently Amended) The method of claim 1 wherein optimizing the programmable logic circuit comprises placing at least one interface buffer in the programmable logic circuit.

7-22. (Canceled)

23. (Currently Amended) A software-to-hardware compiler for optimizing a circuit that implements a program implemented in programmable logic, the compiler configured to:

generate a programmable logic circuit that implements a program;

analyze [[a]] the programmable logic circuit ~~implemented in the programmable logic~~ for ~~possible~~ optimizations, wherein the analyzing comprises determining whether to split the program into a hardware portion implemented in the programmable logic circuit and a software portion implemented in at least one software processor; ~~and~~

optimize the programmable logic circuit into the optimized circuit to provide a more efficient implementation of the program by modifying the programmable logic circuit to ~~executing a~~ execute the software portion of the program ~~using software constructs, wherein using software constructs comprises~~ on the at least one software processor; and

~~establishing~~ establish communications between the optimized programmable logic circuit and the at least one software ~~device~~ processor.

24. (Currently Amended) The software-to-hardware compiler of claim 23 further configured to analyze the programmable logic circuit at a later stage in a compilation.

25. (Currently Amended) The software-to-hardware compiler of claim 23 further configured to analyze the programmable logic circuit's critical path.

26. (Currently Amended) The software-to-hardware compiler of claim 23 wherein optimizing the circuit comprises placing at least one register in the programmable logic circuit.

27. (Currently Amended) The software-to-hardware compiler of claim 23 wherein optimizing the circuit comprises placing at least one FIFO in the programmable logic circuit.

28. (Currently Amended) The software-to-hardware compiler of claim 23 wherein optimizing the circuit comprises placing at least one interface buffer in the programmable logic circuit.

29. (New) The method of claim 1 wherein modifying the programmable logic circuit comprises removing the software portion of the program from the programmable logic circuit.

30. (New) The The software-to-hardware compiler of claim 23 wherein modifying the programmable logic circuit comprises removing the software portion of the program from the programmable logic circuit.